THE CLAIMS

1. (Currently Amended) A method to design an integrated semiconductor product, comprising:

   (a) inputting a description of a range of processing functions into a slice ~~description~~ definition, the slice ~~description~~ definition comprising a transistor fabric, and/or at least one hardmac memory;

   (b) determining if the range of processing functions has a plurality of memory requirements; and

   (c) determining a largest common memory that can satisfy ~~the range of processing functions and~~ the plurality of memory requirements; and

   (d) including the largest common memory into the slice definition.

2. (Original) The method of claim 1, further comprising embedding the largest common memory into the at least one hardmac memory.

3. (Currently Amended) The method of claim 2, further comprising:

   (a) embedding at least one embodiment of the range of processing functions into the slice ~~description~~ definition.

4. (Original) The method of claim 1, further comprising:

(a) generating register transfer logic from the transistor fabric so that one of the range of processing functions can use a first portion of the largest common memory.

5. (Original) The method of claim 4, wherein the register transfer logic further comprises logic for a port to access the first portion of memory used by the one of the range of processing functions.

6. (Original) The method of claim 5, wherein the first portion of the largest common memory to be used by one of the range of processing functions is an instruction cache.

7. (Original) The method of claim 6, wherein a second portion of the largest common memory to be used by one of the range of processing functions contains tags/addresses for instructions in the instruction cache.

8. (Original) The method of claim 6, wherein a second portion of the largest common memory to be used by one of the range of processing functions is a valid register indicating valid and/or invalid instructions in the instruction cache.

9. (Original) The method of claim 4, wherein the first portion of the largest common memory to be used by one of the range of processing functions is a data cache.

10. (Original) The method of claim 9, wherein a second portion of the largest common memory to be used by one of the range of processing functions contains tags/addresses for data in the data cache.

11. (Original) The method of claim 9, wherein a second portion of the largest common memory to be used by one of the range of processing functions is a valid register indicating which data in the data cache is or is not valid.

12. (Original) The method of claim 4, wherein a first portion of the largest common memory to be used by one of the range of processing functions is a tightly coupled memory.

13. (Currently Amended) The method of claim 4, further comprising:

(a) identifying a second portion of the largest common memory not used by one of the range of processing functions;

(b) generating register transfer logic to create an additional function from the transistor fabric;

(c) generating register transfer logic to create an additional register and/or memory from the second portion of the largest common memory;

(d) ~~(c)~~ generating the interconnect register transfer logic to connect the additional register and or memory to the additional function;

(e) ~~(d)~~ adding the interconnect and the generated register transfer logic to the slice ~~description~~ definition.

14. (Original) An article of manufacture, comprising a data storage medium tangibly embodying a program of machine readable instructions executable by an electronic processing apparatus to perform method steps for operating an electronic processing apparatus, said method steps comprising the steps of:

(a) reading a plurality of input files relating to a plurality of embodiments of processing functions that could be incorporated into a design of a partially manufactured semiconductor product having a transistor fabric;

(b) determining the largest common superset of memory that can be used by all of the plurality of embodiments of the processing function;

(c) embedding the superset of memory into the design of the partially manufactured semiconductor product;

(d) generating a plurality of output files to configure the embedded memory superset for use by a selected embodiment of the plurality of processing functions; and

(e) updating the design of the partially manufactured semiconductor product with the output files.

15. (Original) The article of manufacture of claim 14, wherein the output files comprise register transfer logic to tie off any portion of the embedded memory superset not used by the selected embodiment of the plurality of processing functions.

16. (Original) The article of manufacture of claim 14, wherein the output files comprise register transfer logic to convert a portion of the transistor fabric to access the embedded memory superset used by the selected embodiment of the plurality of processing functions.

17. (Original) A method of configuring a partially manufactured semiconductor product having a transistor fabric and embedded with a memory superset capable of satisfying the memory/register requirements of all of a range of processing functions, the method of configuring comprising the steps of:

(a) selecting one processing function from the range of processing functions;

(b) determining how the memory superset is to be apportioned to the selected one processing function;

(c) apportioning the memory superset;

(d) tying off that portion of the memory superset that is not apportioned;

(e) determining how to access the apportioned memory superset;

(f) creating logic within the transistor fabric to access the apportioned memory superset.

18. (Original) A system to design a partially manufactured semiconductor product, comprising:

(a) means to receive a functional description of the partially manufactured semiconductor product;

(b) means to determine if the functional description may include a range of processing functions;

(c) means to evaluate the memory and/or register requirements of the range of processing functions;

(d) means to specify a memory superset configurable for a memory and/or register requirement for all of the processing functions in the range; and

(e) means to embed the memory superset into the partially manufactured semiconductor product.

19. (Original) The system of claim 18, further comprising:

(a) means to configure the memory superset into the memory and/or register requirement for one or more of the processing functions in the range;

(b) means to create the logic necessary to access the memory and/or register requirement for one or more of the processing functions in the range.

20. (Original) A partially manufactured semiconductor product, comprising:

(a) a plurality of functional areas, at least one of the functional areas embedded into the semiconductor product as a configurable superset of semiconductor memory;

(b) at least another of the functional areas reserved for one of a range of processing circuits, each one of the range of processing circuits capable of using all or a portion of the configurable superset of semiconductor memory;

(c) configuration logic capable of fulfilling a memory/register requirement of at least one of the range of processing circuits from the configurable superset of semiconductor memory; and

(d) port logic capable of accessing the memory/register requirement fulfilled from the configurable superset of semiconductor memory.